EXPRESS MAIL LABEL NO:

EL 927 724 634 US

Integrated Circuit Package And Method For Fabrication

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FIELD OF THE INVENTION

This invention relates to semiconductor packages and in particular to a low cost package for one or more integrated circuit chips.

BACKGROUND OF THE INVENTION

A package for an integrated circuit chip protects the integrated circuit chip (sometimes called a "die"), provides conductive leads for allowing electrical signals to be sent to (from) the outside world from (to) the integrated circuit die, and removes heat generated by electrical currents flowing in the circuitry formed in the die.

Satisfaction of these requirements can result in a sophisticated, complicated structure which is expensive to build and which affects the performance of the electrical circuits in the die within the package. There is a need for a semiconductor package which is both low cost and meets the above-described requirements for a semiconductor chip package.

SUMMARY OF THE INVENTION

In accordance with this invention, an integrated circuit die package is provided which embeds at least one integrated circuit die in a substrate. The top surface of the at least one die is substantially coplanar with the top surface of the substrate. Conductive paths are formed from the at least one die to conductive contact points on the substrate. These paths allow electrical signals to be sent from (to) external circuitry to (from) the at least one die.

In one embodiment of the invention, at least one integrated circuit chip is embedded in a substrate with the top surface of the at least one integrated circuit chip being substantially coplanar to the top surface of the substrate. A single layer of conductive material, typically metal, is deposited on the top surface of the embedded

substantially coplanar structure and patterned to form lands or bonding pads on the substrate as well as to form the interconnect to the aforementioned lands or pads on the substrate from bonding pads on the at least one embedded integrated circuit chip. A conductive plane over the at least one integrated circuit chip may also be formed from this single masking operation.

The location of the lands on the substrate may duplicate the footprint of a PQFP, PLCC or other conventional package such as a ball grid array so as to facilitate the use of the package of this invention in existing applications.

In an alternative embodiment, to enhance AC performance, a ground or Vcc plane is created over the at least one silicon die. Conductive traces, typically copper, are created from the respective pads on the silicon die to connect the plane to Vcc, ground, and/or an RF shield. This plane may be created during the same photo-masking operations that create the lands or pads on the substrate and the interconnecting traces as described above.

A dielectric which may be a solder mask or other plastic is formed over the top surface of the substrate so as to encapsulate the finished package, exposing only the lands or bonding pads on the substrate so that these lands may be electrically contacted by lead balls, direct copper connections, or other means. In some applications, similar openings may also be purposely created exposing geometrically defined areas of the ground or Vcc plane to allow the plane to be connected by lead balls, direct copper connections or other means.

As an alternative embodiment, following the placement of lands on the top side of the substrate, lands or bonding pads are created on the reverse side of the substrate so that they align with each of the lands on the top (i.e. front) side. Holes are then drilled mechanically or by laser through each of the lands on the front side and through the underlying substrate to form vias with the matching lands on the reverse (i.e. back) side of the substrate. The vias are then plated, preferably with copper but with any appropriate conducting metal to make them conductive, thus electrically connecting the coinciding front side lands with the backside lands.

In this alternative embodiment, the front and back sides are encapsulated with a solder mask or other plastic as described above with only the lands located on the back side of the substrate opposite the coplanar structure remaining exposed so that these lands may be electrically contacted by lead balls, direct copper, copper formed over a barrier metal such as chrome, connections, or other means to electrically conductive traces or contacts on a printed circuit board or other substrate.

As a feature of this invention, the conductive paths and conductive lands are formed from a single layer of conductive material such as copper or other appropriate metal using standard deposition and photolithographic techniques known in the semiconductor and printed circuit arts. This reduces the package cost while at the same time allowing great flexibility in the location of the electrical pads or lands for transmitting signals to and from the at least one embedded die.

In each of the embodiments described above, the edges of the at least one integrated circuit die can be either substantially perpendicular to the top surface of the die or can be beveled relative to the top surface of the die. Depending on the angle of the bevel, beveled surfaces either lock the embedded die in place in the underlying substrate or help center the die as it is being pressed into a depression or opening in the substrate.

In accordance with another embodiment of the invention, a protective coating is formed over the top surface of the at least one integrated circuit die to act as a barrier between the conductive material that is deposited over the coplanar structures and the die, and to protect at least one integrated circuit die from contaminants. This protective coating may be placed over the at least one integrated circuit die while the die are still part of a whole wafer, prior to sawing or other method of segmenting a silicon wafer into the individual die. Openings in the protective coating are then formed to expose the bonding pads on the silicon die to allow electrically conductive leads to be attached to these bonding pads.

In another embodiment, to prevent leakage currents around the edges of the at least one integrated circuit die, the at least one integrated circuit die is embedded in the substrate material such that the top surface(s) of the at least one integrated circuit die is (are) beneath the adjacent top surface of the substrate by a selected amount sufficient to ensure that the edges of the silicon die are embedded below the surface and completely

surrounded by substrate material. Again, bonding pads on the top surface(s) of the at least one integrated circuit die are connected by conductive paths to lands or bonding pads formed on a selected surface. The lands or bonding pads on the substrate are, in some embodiments formed simultaneously with, and from the same conductive materials as the conductive paths. The resulting structure then can be applied directly to a printed circuit board by placing the exposed bonding pads on the substrate directly over corresponding contacts on the printed circuit board. Typically, solder balls formed on the bonding pads on the substrate allow electrical contact to be made between these bonding pads and the electrical contacts on the printed circuit board.

The die package of this invention is inexpensive to manufacture compared to prior art packages, provides a thinner package than in the prior art and controls impedance associated with the conductive leads interconnecting the die to the outside world.

This invention will be more fully understood in light of the following detailed description taken together with the following drawings.

DESCRIPTION OF THE DRAWINGS

Figs. 1a and 1b show in cross-section a semiconductor integrated circuit die embedded in a substrate of a heat moldable material such as a plastic or a combination of plastics to form a unitary integrated structure.

Figs. 2a and 2b show the top view of the structure of Fig. 1 wherein an integrated circuit chip 21 with a plurality of bonding pads 22 formed on the top surface thereof has a plurality of conductive paths 23 leading from the integrated circuit chip bonding pads 22 to bonding pads 24 formed on the top surface of the substrate in which chip 21 is embedded.

Figs. 3a and 3b show the structure of Fig. 2a and a cross-section of this structure, respectively, the cross-section showing the structure of Fig. 3a upside down ready to be mounted on a printed circuit board using solder balls 25 formed on top of bonding pads 24 to provide the electrical connection between the die 21 and the electrical circuitry on the printed circuit board.

Figs. 4a and 4b show an embodiment of the invention wherein the integrated circuit chip 21 contains over the top surface thereof a protective layer 29.

Figs. 5a and 5b show an embodiment of the invention wherein conductive lands or conductive pads are placed on the surface of the substrate opposite to the surface in which the die in mounted and conductive vias are formed through the substrate to connect the electrically conductive paths from the conductive pads on the top surface of the die to these conductive lands.

DETAILED DESCRIPTION

The following detailed description is illustrative only and not limiting. Other embodiments of this invention will be obvious to those skilled in the art in view of this description.

Figs. 1a and 1b illustrate an integrated circuit chip 14 embedded in a substrate 11, typically of plastic, but of any other non-conductive material, including a combination of plastics, which is heat deformable and therefore capable of having die 14 pressed into material 11 when heated to form the structure shown in Figs. 1a and 1b. More than one integrated circuit chip can be embedded in substrate 11, if desired. Die 14 has a top surface 17 on which are formed a plurality of electrically conductive bonding pads 13 of which bonding pads 13-1 and 13-2 are shown. Top surface 17 of die 14 is approximately coplanar with top surface 18 of substrate 11. Consequently, conductive leads such as conductive material 12 can be formed from a bonding pad such as pad 13-2 on the top surface of die 14 over the top surface of substrate 11 to end in a bonding pad (not shown) on substrate 11. Overlying the top surface 18 of substrate 11 and the top surface 17 of die 14 can be a protective layer of an overcoating material to protect the top surface of die 14 and the conductive leads 18 from moisture and other contaminants.

The silicon die 14 embedded in substrate 11 is placed in substrate 11 by heating substrate 11 until the plastic material making up substrate 11 is easily deformable and then pressing the die 14 gently into the plastic material until the top surface 17 of the die 14 is approximately coplanar with the top surface 18 of the substrate material 11. Techniques for doing this are described in copending U.S. patent application Serial Number 09/963,337 filed September 24, 2001 and assigned to JigSaw Tek, Inc., the

assignee of this application. Application Serial Number 09/963,337 is incorporated herein by reference in its entirety. The edges 16-1, 16-2 of die 14 in Fig. 1a are shown to be substantially perpendicular to the top surface of the integrated circuit die 14. However, die edges 15-1 and 15-2 in Fig. 1b are shown to be tapered either to allow die 14 to be more easily pressed into the flowable plastic material 11 or to lock the die 14 into the plastic substrate 11 once the plastic cools and solidifies. Dashed lines 19-1 and 19-2 in Fig. 1b show how the edges 15-1 and 15-2 can be tapered outward to lock die 14 in the substrate 11.

Figs. 2a and 2b show a top view and cross-sectional side view, respectively, of an integrated circuit chip 21 embedded in substrate 20 in accordance with this invention. Of course, more than one integrated circuit chip 21 can be embedded in substrate 20 if desired. Die 21 has a plurality of bonding pads 22-1 through 22-60 formed on the top surface thereof in a well-known manner. The top surface 27 of die 21 as shown in cross-section Fig. 2b is slightly below the top surface 28 of substrate material 20. The fact that the top surface 27 of die 21 is slightly below the top surface 20 of substrate 20 allows a protective material 29 to be placed on top surface 27 of die 21 and have the top surface of the protective material be coplanar with the top surface of the substrate. However, the top surface 27 of die 21 is still considered to be substantially coplanar with the top surface 28 of the substrate material 20 even with this protective material 29 formed on the top surface 27 of die 21.

As shown in Fig. 2a, electrically conductive paths 23-1 through 23-60 are formed to connect each of the bonding pads 22-1 through 22-60, respectively, on the top surface 27 of die 21 to a corresponding one of bonding pads 24-1 through 24-60 on the top surface 28 of substrate material 20. Preferably bonding pads 24 are formed simultaneously with and from the same layer of material as electrically conductive paths 23. Bonding pads 24-1 through 24-60 can have formed on their top surfaces conductive balls 25-1 through 25-60 (of lead or other conductive material) to allow pads 24-1 through 24-60 to be electrically connected to electrically conductive traces on a substrate or printed circuit board to which the structure shown in Figs. 2a and 2b will be functionally connected. The electrically conductive traces on the printed circuit board or substrate can then conduct the electrical signals from die 21 to other appropriate circuitry on the printed circuit board or substrate or from such other circuitry to die 21. Such other

circuitry can include devices packaged as shown in Figs. 2a and 2b or other more conventionally packaged structures, all within the discretion of the circuit designer.

As shown in application Serial No. 09/963,337, die 21 is embedded in substrate material 20 by heating the substrate material 20 until material 20 is deformable and easily flowable and then pressing die 21 into the top surface of material 20.

Substrate 20 can be any appropriate plastic material or combination of plastic materials which is deformable by heating. The structure shown in Fig. 2b has formed over the top surface 27 of die 21 and the top surface 28 of substrate material 20 a plastic overcoating 26 to protect the top surface of die 21 and substrate material 20 from moisture and other contaminants which might affect the electrical performance of the die 21. Plastic coating 26 is formed after electrically conductive paths 23 and bonding pads or lands 24 have been formed on the top surface 28 of substrate material 20 to connect to bonding pads 22 on the top surface 27 of die 21. Openings are provided in coating 26 to expose the tops of lands 24. Coating 26 can also be formed of polyimide, any other appropriate polymer (including photosensitive polymers), or an appropriate insulating layer.

Conductive paths 23 and bonding pads 24 are typically formed using well-known photolithographic techniques. To do this, a layer of electrically conductive material, typically a metal such as copper, is deposited in any one of several well known ways (for example, by evaporation or sputtering) on the top surfaces 27 of die 21 and 28 of substrate material 20. This layer is then patterned to form the conductive paths 23 and bonding pads or lands 24 using photoresist and etching techniques, both well known in the art. Bonding pads 24 can be formed to match spatially the electrical contacts or leads on any one of several different package types (such as PQFP, PLCC or other conventional package type to allow the package of this invention to be used in place of such a conventional package with no change in the printed circuit board layout).

Figs. 3a and 3b show the structure of Figs. 2a and 2b with the cross-sectional view in Fig. 3b showing the semiconductor die 21 embedded in substrate material 20 (typically a plastic or a combination of plastics deformable at elevated temperatures) but with the resulting structure upside down ready to be mounted on a printed circuit board or substrate to interconnect the pads 22 on the top surface 27 of die 21 to the circuitry on the

printed circuit board or substrate (neither of which are shown) using electrically conductive paths 23 from electrically conductive pads 22 to electrically conductive pads 24 on the top surface 28 of substrate 20. Lead solder balls 25 interconnect bonding pads 24 to other circuitry mounted on the printed circuit board or substrate.

Figs. 4a and 4b show the structure of Figs. 2a, 2b, and 3a, 3b with a protective plastic coating 29 formed over the top surface 27 and bonding pads 22 on die 21. Plastic protective coating 29 prevents moisture and other contaminants from reaching the surface of die 21 and thereby protects the electrical performance of the die.

Traces 23 and pads or lands 24 in the structures described in Figs. 2a, 2b, 3a, 3b and 4a, 4b typically can be of copper or any other appropriate conductive material, including composite layers of conductive materials. The conductive material is deposited by any appropriate technique in a manner so as not to adversely affect the underlying substrate. Formation of these traces from a single layer of conductive material such as metal using standard photolithographic techniques (i.e. masking the metal with photoresist, patterning the photoresist to expose the portions of the metal layer to be removed, removing the exposed metal, and then removing the masking photoresist to leave the resulting conductive paths and pads) will result in finely formed traces and lands of the type shown in the top views of Figs. 2a, 3a and 4a. The partial plastic overcoat 29a in Fig. 4b contrasts with the full plastic overcoat 26 shown in Fig. 2b. Both methods are commercially used today to protect integrated circuits contained within a package.

Referring, for example, to Figs. 2a, 3a, and 4a, the silicon die 21 shown in these figures can have formed thereon a coating of electrically conductive material over its top surface. Such a coating would be formed in the boundary shown in Fig. 3a by the dashed lines 31 to provide a ground plane or a VCC plane. Such a plane can function either as an isolator or an RF shield. Selected portions of such a conductive layer would be connected to selected one or more of bonding pads 22-1 through 22-60 to provide the desired electrical bias. In an alternative embodiment, not shown in the drawing, a protective coating (such as coating 26 as described above) is formed over the conductive plane, a plurality of openings are created in coating 26 over the plane to allow solder balls to be attached, or direct copper connections to be made to the plane. These connections may be used to electrically connect the plane to an external substrate such as a printed circuit

board, provide added mechanical strength and can also be utilized to provide thermal paths for removing heat from the integrated circuit.

As an alternative embodiment, not shown in any of the drawings, a layer of electrically conductive material may be formed on the side opposite the silicon die, and may or may not be electrically connected to ground or Vcc, and may provide additional thermal conduction or RF shielding. This plane may be in addition to a plane formed on the same side as the silicon die.

Figs. 5a and 5b shown an alternative embodiment of this invention wherein integrated circuit die 21 is embedded in substrate material 20 (typically plastic or a combination of plastics, all heat deformable to allow die 21 to be pressed into the substrate material 20), together with vias 51-1 through 51-60 (of which only 51-23 and 51-53 are shown) formed through substrate material 20 to allow the packaged integrated circuit die 21 to be mounted on a printed circuit board with the top surface 17 of die 21 facing outward from the printed circuit board. Bonding pads 54-1 through 54-60 are formed on the bottom surface 57 of substrate material 20 and solder balls 55-1 through 55-60 are then formed on the corresponding ones of bonding pads 54-1 through 54-60 to allow the structure to be interconnected to an underlying PC board. Vias 51-1 through 51-60 (of which vias 51-23 and 51-53 are shown in cross-section Fig. 5b) are formed in any one of several ways. Typically, such vias can be formed by burning openings through conductive material 20 with a laser or forming such openings with a mechanical drill at the selected points where the vias 51 are to be present and then filling these vias using electroless plating with an electrically conductive material such as copper. Then, following the formation of the vias, the top surface 17 of integrated circuit die 21 and the top surface 18 of substrate 20 have formed thereon conductive paths 23 in the manner described above in conjunction with Figs. 2a, 3a and 4a. A protective coating 26 is formed over the top surface of both die 21 and substrate 20 to protect both the die and the electrically conductive leads 23 (of which only conductive leads 23-3 and 23-53 are shown in cross-section in Fig. 5b) from moisture and other contaminants which might interfere with the electrical performance of the circuitry. Such interference can come about in a number of ways including the formation of conductive paths between adjacent conductive leads or the corrosion of conductive paths due to the presence of unwanted contamination.

The semiconductor package of this invention is simple and inexpensive to make. The use of a single layer of electrically conductive materials to form conductive paths and lands on the surface of the composite substrate-die structure yields a rugged inexpensive, ultra-thin structure. The structure of this invention is essentially a planar structure. Therefore, two or more such structures can be stacked one on top of the other with appropriate connections being formed between the stacked packages to allow multichip modules to be fabricated with a small footprint in compact volumes.

The integrated circuit chip or die used with the disclosed structure will typically be silicon but could also be of any other semiconductor material such as gallium arsenide or germanium. An advantage of this invention is that die of the same or different materials can be included in one package and interconnected to each other and the outside world by conductive traces formed as described above. Of course, a conductive trace connecting two die would run from a bonding pad on the top surface of one die to a bonding pad on the top surface of the other die.

Unless otherwise specified, the term "conductive" as used herein means "electrically conductive." An electrically conductive material can also conduct heat and in certain embodiments serves that function as well, as described above.

While several embodiments of this invention have been described, other embodiments of this invention will be obvious in view of this disclosure.